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Analysis of Process Flow for n Type TUNNEL FET Using TCAD Process and Device Simulation

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Abstract— **This paper deals with the reduction and simplification of process steps for a tunnel FET using process simulation in Synopsys TCAD. The simulation has been performed by reducing many masking steps as well as eliminating other steps like halo implantation, LDD implantation etc. without performance degradation. The simulated result shows that the proposed tunnel FET is feasible to be fabricated in advanced MOS technology.**

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Keywords—MOS technology; process steps

I. INTRODUCTION

The reduction of size of MOSFET devices has improved the packing density as well as it has mitigated the ITRS requirement[1]. But as the devices shrink, the number of process steps increases, also the manufacturing time and manufacturing cost increases. So process step reduction is very important considering manufacturing time and cost[2]-[3]. Also the device performance should not be hampered.

In this paper process steps has been performed for a silicon tunnel FET using TCAD santaurus process[4]-[5]. It is a powerful tool in which the process flow is simulated by issuing a sequence of commands that corresponds to the individual process steps. Process simulation output includes the structural profile. Also the structural and electrical parameters of the device can be extracted by using the TECPLOT. Structural information of the device is described the doping profile.

After the process simulation, device simulation has been performed to analyze the behavior of the proposed structure. $I_D - V_{GS}$ curve has been extracted.

II. PROCESS SIMULATION

A. Selection of Substrate

The simulation starts with a block of Silicon wafer as substrate material. The length and breadth of the silicon substrate is 100nm and 30 nm respectively. Then the substrate is doped with Phosphorous at900 ^oC with original concentration of $1x15cm^{-3}$.The wafer orientation has been set to (100)

B. Gate oxide growth

a very thin highly controllable oxide layer has been grown up on the surface of top silicon film by thermal oxidation as a buffering layer. Here, the wafer is exposed to the oxidizing gases for 20 minutes at an ambient temperature of 900°C. The pressure of the ambient gas has been set to 1 atm, and the flows of oxygen and nitrogen are set to 1.2 l/minute and 1.0 l/minute, respectively.

C. Poly Silicon deposition

11 nm of polysilicon is deposited over the entire structure. The layer is grown in the vertical direction only. The poly silicon is heavily doped with 10^{20} cm^{-3} to reduce the sheet resistance so that RC time constant can be improved. The advantage of taking polySilicon as gate electrode is its ability to use as further mask for precisely defining source and drain.

D. Gate definition

The polysilicon length has been kept small so that resistance is small as resistance is directly proportional to length. So the time constant RC decreases. A mask has been defined to protect the gate area. Also a positive photoresist layer has been deposited with minimum thickness outside the mask. There has been minimum overlap between gate and source as well as

gate and drain area. This has been performed not to extend source and drain under gate.

E. Polysilicon and Oxide etch

Anisotropic etching has been performed because it etches material away in a direction that is purely vertically downwards. In the etching process the exposed part of the polysilicon has been removed and later on the oxide has been removed by repeating etching process in which poly silicon has been by default used as mask. Etching depth has been taken larger than the deposited layer to ensure that no residual material remains. Then all the photo resists has been removed

F. Formation of source, channel and drain

The source, channel and drain region has been defined by refine box. Ion implantation has been used for doping the impurity atoms in to the active regions. Because shallower junctions are produced which are compactable with small dimension process. This reduces overlap between the regions. Then Boron ions were implanted into source region. Its concentration was at the order of 10^{21} cm^{-3} with implantation energy of 160KeV and tilted implantation angle of 0 rad. In the similar way channel has also been doped with Boron with a concentration of 10^{17} cm-3 and the drain is doped with Arsenic having concentration $5x10^{19}cm^{-3}$.The source-to-channel doping has been heavy and abrupt that causes bandgap narrowing. As a result tunneling probability increases and on-current maximizes.

G. Preparation of gate electrodes

Once device layers are completed, photolithographic process has been adopted to form source, drain and gate contact holes. Then the corresponding electrodes has been prepared by deposition of a 1nm-thick Aluminum film following metals etching.

The cross section view of complete device cell is illustrated in Fig.1

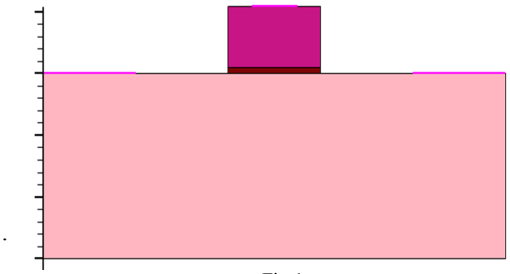

Fig.1

Simulation is done using Synopsys TCAD Tools based on non local mesh band-to-band tunneling model. Doping dependent mobility model has been used. Band gap narrowing has also been activated. The total drain current vs gate voltage has been measured for the proposed device. No performance degradation is observed by this process.

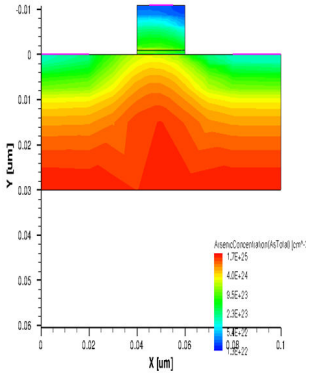

Fig. 2

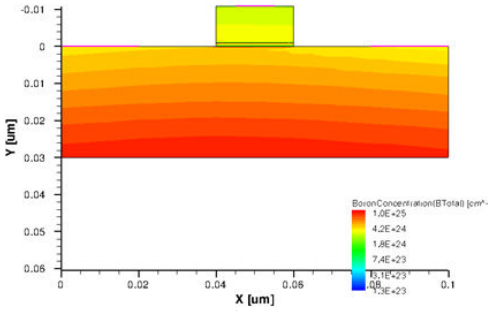

Fig. 3

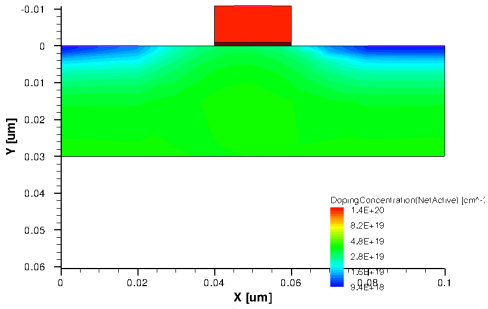

Fig. 4

The silicon layer is assumed to have initially a uniform phosphorus concentration of $1x10^{15}$ cm^{-3}. However, due to the collision of all dopants (arsenic, phosphorous, and boron) with point defects as well as among themselves via the electric field of the charge impurities results in the concentration distribution which is quite non-uniform after the

activation/annealing as shown in Fig.2, 3 and 4. The I_D-V_{GS} characteristics of the proposed device is shown in Fig. 5 .The on current is in the range of 0.8mA and OFF current 10^{-9} A. This meets the ITRS requirement.

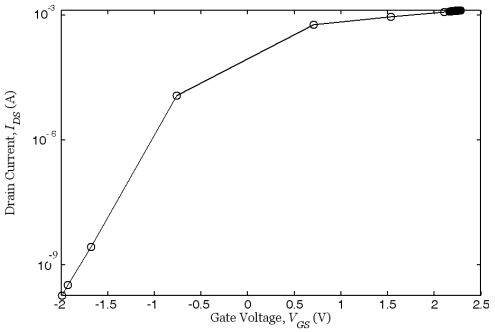

Fig. 5

III.CONCLUSION

The device is fabricated with simplified process steps and the proposed tunnel FET can be using advanced CMOS technology. Moreover, the I_D-V_G characteristics of the device also meets the ITRS requirement.

Acknowledgement

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